

ABSTRACT OF THE DISCLOSURE

A memory cell array of a semiconductor memory device includes a first sub array configured by a plurality of first cell units, a second sub array configured by a plurality of second cell units, and a non-memory cell region used for a backgate and arranged between the two sub arrays. Memory cells located on each side of the non-memory cell region are oriented in the same direction. Pairs of bit lines have substantially the same number of bit line contacts.